PCT/IB04/51080
ML030806

Europäisches Patentamt | European Patent Office | Office européen des brevets

Bescheinigung | Certificate | Attestation

Die angehefteten Unterlagen stimmen mit der ursprünglich eingereichten Fassung der auf dem nächsten Blatt bezeichneten europäischen Patentanmeldung überein.

The attached documents are exact copies of the European patent application described on the following page, as originally filed.

Les documents fixés à cette attestation sont conformes à la version initialement déposée de la demande de brevet européen spécifiée à la page suivante.

Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

03102062.1

PRIORITY DOCUMENT
SUBMITTED OR TRANSMITTED IN
COMPLIANCE WITH
RULE 17.1(a) OR (b)

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

R C van Dijk

Anmeldung Nr:
Application no.: 03102062.1
Demande no:

Anmeldetag:
Date of filing: 09.07.03
Date de dépôt:

Anmelder/Applicant(s)/Demandeur(s):

Koninklijke Philips Electronics N.V.
Groenewoudseweg 1
5621 BA Eindhoven
PAYS-BAS
Philips Intellectual Property & Standards
GmbH
Steindamm 94
20099 Hamburg
ALLEMAGNE

Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
Si aucun titre n'est indiqué se referer à la description.)

Integrated circuit testing

In Anspruch genommene Priorität(en) / Priority(ies) claimed /Priorité(s) revendiquée(s)
Staat/Tag/Aktenzeichen/State/Date/File no./Pays/Date/Numéro de dépôt:

Internationale Patentklassifikation/International Patent Classification/
Classification internationale des brevets:

G01R31/28

Am Anmeldetag benannte Vertragstaaten/Contracting states designated at date of filing/Etats contractants désignées lors du dépôt:

AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LI LU MC
NL PT RO SE SI SK TR

Integrated circuit testing

The present invention relates to the field of integrated circuit (IC) testing.

During fabrication, and particularly at the end of a production cycle, an IC is tested to ensure its quality and functionality. If, at any point during the production cycle, an IC is found not to function correctly, or has operating parameters which fall outside specified ranges, it may be discarded in order to save time and money.

Such tests must be cheap and efficient, and must use as little specialized test equipment as possible in order to minimize test costs.

In addition to tests to determine functionality, other tests are also performed in order to ascertain certain operating parameters of an IC such as maximum and minimum operating voltage and/or temperature, and maximum and minimum applicable clock frequencies, for example.

These tests enable the 'characterization' of the IC, and are also performed with expensive test equipment. The characterization enables the specification of the IC product to be readily available for a consumer, enabling them to determine a device's suitability for a particular application. Any characterization carried out must, therefore, be correct, and is an important part in the production cycle of integrated circuit devices.

Due to costs, not every IC is characterized, however. In the current process technologies this is still acceptable. In future technologies, however, the process spread will increase in such a way that dies on a single wafer will get different physical parameters, and therefore characterizing every IC will become mandatory in order to ensure a good quality product. In this case, characterization must be cheap enough so that it may be able to be applied to every IC.

Figure 1 shows the results of a typical characterization process carried out using expensive test equipment. Figure 1 is a so-called 'Shmoo plot', which shows a characterization of the frequency of an IC versus supply voltage of the IC in question.

Specifically, a Shmoo plot, as exemplified by figure 1, is a graph which represents how a particular test passes or fails when parameters like frequency, voltage, or

temperature are varied and the test is executed repeatedly on the IC in question. The shape of the failing region is meaningful and helps in determining the cause of the failure. In the Shmoo plot of figure 1, a pass is shown as a white square, and a fail is shown as a grey square. A Shmoo plot of a normal circuit operation shows better high-frequency performance as supply voltage increases, as shown in figure 1.

In order to make characterization tests viable, they must be performed quickly, and utilize as little test equipment as possible. However, as mentioned, due to increasing process shifts (even on a single wafer) for new semiconductor IC technologies, a characterization test is unlikely to produce the same results (i.e. operating parameters) for every IC. However, in order to ensure low production costs, it is not practicable to separately characterize every IC at the end of its production process using the test equipment.

US 2001/0035766 (to Nakajima) discloses a method and a device for providing a characterization of a device (or product). The Nakajima document discloses that the method may be implemented into an IC test device. This embedded device is separate from the device to be tested, however, and therefore does not overcome the current characterization problems as the method and device of the Nakajima patent is directed towards the characterization of another device.

There is therefore a need for a method and system which is able to provide cost effective and space efficient characterization of ICs and which obviates the need for separate, expensive and/or extensive test equipment, and which provides reliable characterization data for each IC.

According to an aspect of the present invention there is provided a semiconductor device characterized by an integral characterization unit operable to provide characterization data for the device.

According to an aspect of the present invention there is provided a method of characterizing a semiconductor device comprising a functional device characterized by providing an integral characterization unit in the semiconductor device, and obtaining characterization data from the integral characterization unit.

Figure 1 is a Shmoo plot for a device under characterization;

Figure 2 shows an IC architecture according to an aspect of the present invention;

Figure 3 shows an IC architecture according to another aspect of the present invention;

Figure 4 shows an IC architecture according to another aspect of the present invention;

Figure 2 shows an IC 201 having an architecture according to an aspect of the present invention.

A supply voltage and clock signal of the IC 201 are controlled by a voltage controller 203, and a clock controller 205 respectively. According to an aspect of the present invention, the voltage controller 203 is operable to provide a variable voltage supply to a device under characterization (DUC) 207, whilst the clock controller 205 is operable to provide a variable clock signal to the DUC 207 (i.e. a clock signal with a variable period). The controllers 203, 205 may usefully be described as 'characterization parameter controllers' to describe their function as controllers which are operable to control a characterization parameter of the DUC 207.

A test interface is provided in order to supply instructions to the controllers 203, 205. In the implementation of figure 2, a hardware or software controller is available outside of the IC 201 in order to execute a characterization. Test stimuli are applied to the DUC 207 externally through an interface. The clock controller 205 is also operable to output the clock signal from the IC 201 in order to synchronize the test stimuli and responses thereto to the external world.

Specifically, the implementation of the system of figure 2 requires a test interface which is operable to provide the voltage controller 203 and the clock controller 205 with the required parameters in order to start a characterization process. The DUC 207 is provided with the test stimuli from an external hardware or software source through a further interface.

The DUC 207 provides the functionality of the IC 201, and all other parts of the IC 201 such as the voltage controller 203 and the clock controller 205 are ancillary items providing test functionality on the IC 201 in accordance with the present invention.

The combination of supplying test stimuli and variable voltage and clock signals via the voltage and clock controllers 203, 205 respectively allows the DUC 207 to be

characterized with respect to the parameters controlled by the controllers 203, 205. In the example shown in figure 2, the parameters used to perform the characterization are therefore voltage and clock period. It will appreciated, however, that any parameter suitable for forming a characterization of a DUC 207 may be controlled by the controllers 203, 205.

In this manner, IC characterization may be performed 'on-chip', thereby providing a built-in chip characterization (BICC) system.

Figure 3 shows an IC 301 having an architecture according to a second embodiment of the present invention. A device under characterization 303 (DUC) is surrounded by built-in self test (BIST) hardware 305 that is operable to generate test stimuli and observe the responses. The use of BIST is well known in the art. The present invention is not directly concerned with BIST, and this will not therefore be described in any further detail.

A supply voltage and clock signal of the IC 301 are controlled by a voltage controller 307, and a clock controller 309. As in the previous embodiment, voltage controller 307 is operable to provide a variable voltage supply to both the DUC 303, and the BIST hardware 305, whilst the clock controller 309 is operable to provide a variable clock signal to the DUC 303. The clock signal is also supplied to the BIST hardware 305. Both the controllers 307, 309 are controlled by the use of external software or hardware control means (not shown). The controllers 307, 309 receive data through a test interface of IC 301.

As before, the DUC 303 provides the functionality of the IC 301, and all other parts of the IC 301 such as the BIST hardware 305, the voltage controller 307 and clock controller 309, are ancillary items providing test functionality on the IC 301.

In the implementation of figure 3, an external hardware or software controller is used to execute a characterization process. Test stimuli are generated internally via the BIST module 309. The test results are output through the test interface.

In a similar manner to the system of figure 2, the controllers 307, 309 are operable to vary a characterization parameter of the DUC 303. For each value of the characterization parameter, a test is performed on the DUC 303. In this manner, characterization of the DUC 303 is performed, the results of which are output from the IC as explained above. The results may be used to generate a Shmoo plot similar to that shown in figure 1, so as to provide a characterization of the DUC 303 with respect to the parameters controlled by controllers 307, 309 (i.e. voltage and clock period respectively in the example of figure 3).

The implementations of figures 2 and 3 provide BICC functionality, but requires the use of an external (to the IC 201, 301) software or hardware. In this way, IC area may be saved as an internal global control module is not required.

Figure 4 shows an IC 401 according to another embodiment of the present invention. In figure 4, the BICC system comprises a voltage controller 403, a clock controller 405, a DUC 407, and BIST functionality provided by BIST hardware 409, similar to that shown in figure 3.

A test interface is provided in order to supply instructions to a global controller 411. In one method of operation, the global controller 411 receives a prompt through the test interface in order to start a characterization process. The prompt can include a request to the global controller 411 to begin the process, and can also include the parameters of the chip 401 that are to be characterized during the process.

Upon reception of this prompt data, the controller 411 is operable to vary certain parameters of the chip 401 via the use of the controllers 403, 405 (which in this case control a voltage and clock signal respectively).

Specifically, the global controller 411, after having received the necessary prompt and characterization parameters through the test interface, is operable to vary certain parameters of the DUC 407 via the use of the controllers 403, 405. In the example shown in figure 4, controllers 403, 405 control a voltage and clock signal of the DUC 407 respectively, and will therefore enable a characterization of the DUC 407 to be performed with respect to IC supply voltage and clock frequency. Such a characterization is usefully depicted in the form of a Shmoo plot as described above with reference to figure 1.

The global controller 411 is operable to program the controllers 403, 405 repeatedly so that a 'virtual' Shmoo plot may be generated.

The implementation of the present invention as exemplified by figures 2 and 3 also advantageously enables the generation of a 'virtual' Shmoo plot, but instead of the global controller providing the characterization parameter controllers with data, this is provided through a test interface from software or hardware.

If BIST is used (figures 3 and 4) in the characterization process, the Shmoo plot will only have pass/fail information. If, however, no BIST is used (figure 2), the Shmoo plot may also contain the number of faults per test. In general, however, the virtual Shmoo plots as generated by the characterization process of the present invention are the same as those generated using external test equipment. As is necessary for Shmoo plots generated by

the test equipment, external software is required in order to be able to view and evaluate the Shmoo plots.

It will be appreciated by those skilled in the art, that although the present invention is being described with reference to voltage and clock controllers, any suitable parameter of the DUC 403 may be controlled by controllers 403, 405. The use of voltage and clock controllers is not intended to be limiting, and is merely included in order to better explain the inventive concept and particular advantages brought forth by the present invention.

If there are memory modules 413 available on the IC 401, it is possible to save the generated Shmoo plot in memory so that it may be read out at the end of the Shmoo plot generation. This will enable the characterization process to be sped up since clock/voltage data will not need to be output from the IC following every measurement cycle.

If, however, no memory modules are available, characterization information is output directly via the test interface.

It will be appreciated by those skilled in the art that the examples given above with reference to, and as shown in figures 2 to 4 are presented in order to better explain the inventive concept embodied by the present invention, and are not intended to be limiting. In particular, it will be appreciated that alternative implementations of the present invention not explicitly mentioned herein are possible. Specifically, the exact nature of tasks performed on- and off-chip (which dictates the number of control and test modules present on the chip) may be varied in order to suit a particular application, or to save chip space, for example. The implementations explained above with reference to the figures merely, therefore, present three specific examples of IC architectures according to the inventive concept of the present invention.

CLAIMS:

1. A semiconductor device (201) comprising a functional device (207) characterized by an integral characterization unit (203) operable to provide characterization data for the device (201).

2. A semiconductor device (201) as claimed in claim 1, wherein the integral characterization unit (203) is operable to provide a control signal to control an operating parameter of the device (201).

3. A semiconductor device (201) as claimed in claim 2, wherein the integral characterization unit (203) is operable to provide a control signal to control a voltage supply of the device (201).

4. A semiconductor device (201) as claimed in claims 2 or 3, wherein the integral characterization unit (203) is operable to provide a control signal to control a clock signal of the device (201).

5. A semiconductor device (201) as claimed in any one of claims 1 to 4, wherein the functional device (207) is operable to receive test data.

6. A semiconductor device (201) as claimed in claim 5, wherein the functional device (207) is operable, in response to said test data, to produce a test response.

7. A semiconductor device (201) as claimed in claim 5 or 6, wherein the functional device (207) is operable to receive a control signal from said integral characterization unit (207).

8. A semiconductor device (201) as claimed in claim 4, wherein the integral characterization unit (203) is operable to provide the clock signal externally to said device (201).

9. A semiconductor device (201) as claimed in any one of the preceding claims, comprising a test interface, and wherein the integral characterization unit (207) is operable to receive data through the test interface.

10. A semiconductor device (201) as claimed in any one of the preceding claims further including software control means operable to provide control data to the integral characterization unit (207).

11. A semiconductor device (201) as claimed in any one of the preceding claims further including hardware control means operable to provide control data to the integral characterization unit (207).

12. A semiconductor device (201) as claimed in claim 10 or 11, wherein the control means is operable to provide control data to the integral characterization unit (207) through a test interface of the device (201).

13. A semiconductor device (301) as claimed in claim 5, further including built in test hardware (305) operable to provide test data to the functional device (303).

14. A semiconductor device (301) as claimed in claim 13, wherein the built in test hardware (305) is IEEE 1149.1 compliant.

15. A semiconductor device (301) as claimed in claim 13 or 14, comprising a test interface and wherein the built in test hardware (305) is operable to receive test data through a test interface of the device (301).

16. A semiconductor device (301) as claimed in any one of claims 13 to 15, wherein the built in test hardware (305) is operable, in response to said test data supplied to said functional device (303), to provide test response data.

17. A semiconductor device (301) as claimed in claim 16, wherein the built in test hardware (305) is operable to output said test response data from the device (301).

18. A semiconductor device (401) as claimed in any one of the preceding claims further including a memory module (413) which is operable to store characterization data of the device (401).

19. A semiconductor device (401) as claimed in any one of the preceding claims, further including a controller (411) which is operable to provide control data to the integral characterization unit (407).

20. A semiconductor device (401) as claimed in claim 19 when appended to claim 13, wherein the controller (411) is operable to provide control data to the built in test hardware.

21. A semiconductor device (401) as claimed in claim 19 when appended to claim 18, wherein the controller (411) is operable to communicate with the memory module (413).

22. A semiconductor device (401) as claimed in claim 19, wherein the controller (411) is operable to receive data over a test interface of the device (401).

23. A method of characterizing a semiconductor device (201) comprising a functional device (207) characterized by providing an integral characterization unit (203) in the semiconductor device (201), and obtaining characterization data from the integral characterization unit (203).

24. A method as claimed in claim 23, further comprising providing a control signal to control an operating parameter of the device (201).

ABSTRACT:

A system and method for providing a built-in characterization of a semiconductor device. The device is provided with a built-in, integral, characterization unit which allows characterization of the device without the need for external test equipment.

Fig. 2

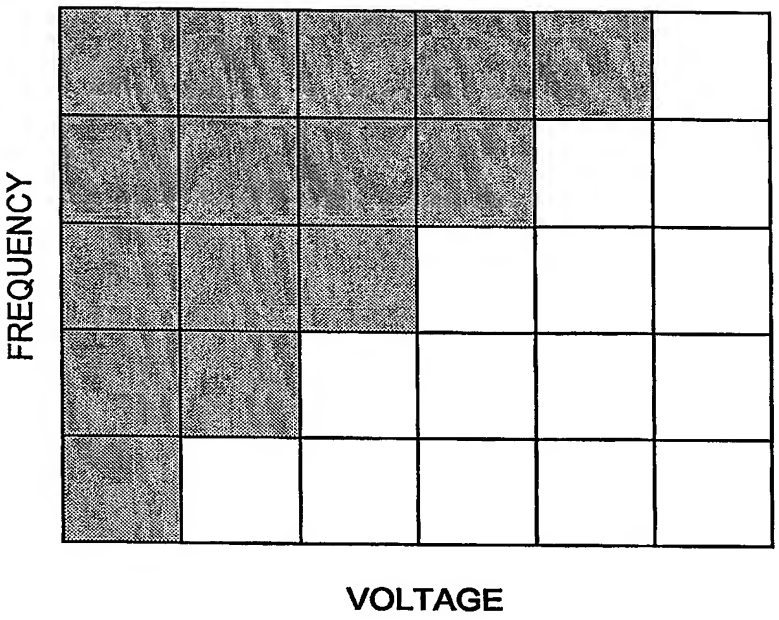

FIG.1

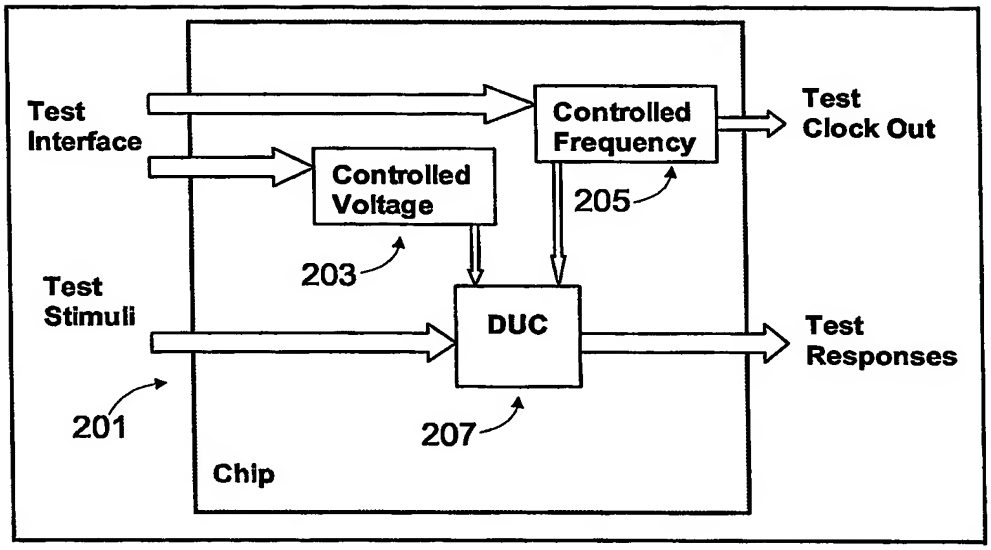
Test
Interface
Controlled
Frequency
Test
Clock Out
Controlled
Voltage
205
203
Test
Stimuli
DUC
Test
Responses
201
207
Chip

FIG.2

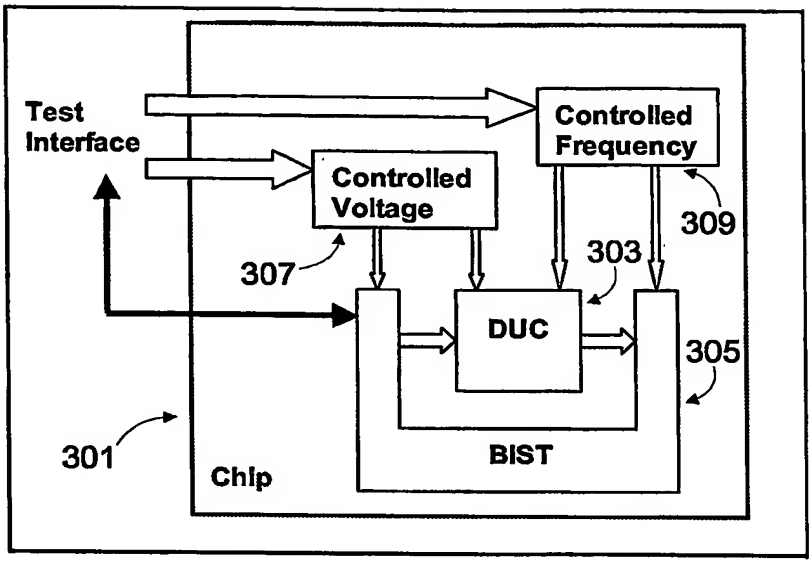
Test
Interface
Controlled
Frequency
Controlled
Voltage
309
307
303
DUC
305
301
Chip
BIST

FIG.3

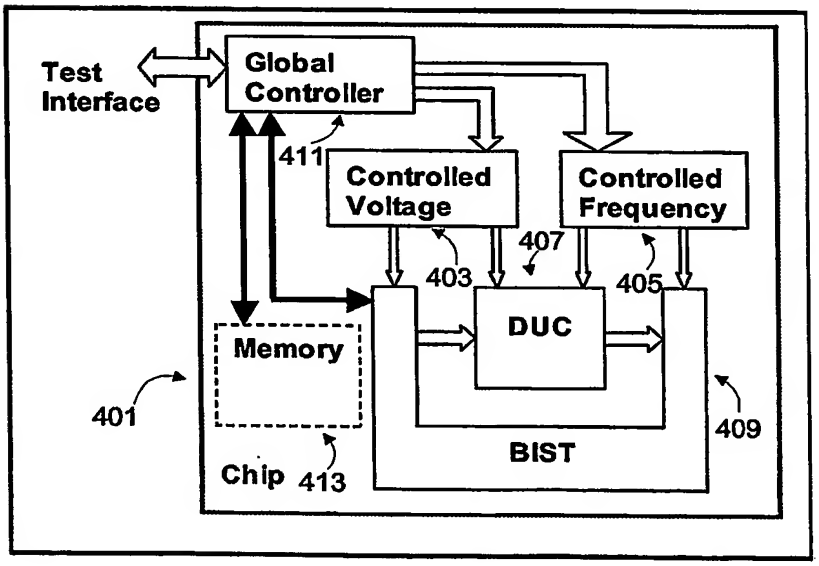
Test
Interface
Global
Controller
411
Controlled
Voltage
Controlled
Frequency
407
403
405
DUC
Memory
401
409
BIST
Chip
413

FIG.4